REMARKS/ARGUMENTS

The office action of August 25, 2004 has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested. Claims 1-42 remain pending in this application. Claim 10-12 and 15-20 have been withdrawn.

Preliminarily, applicants note with appreciation the indication that the application contains allowable subject matter. Specifically, claims 14, 27, 31 and 42 have been objected to for being dependent upon a rejected base claim, but would be allowable if amended to incorporate all the features of their ultimate base claim and any intervening claims.

The drawings stand objected to under 37 C.F.R. § 1.83(a) for failing to show transistors having different gate oxide thickness as described in the specification. Figs. 16A and 16B have been amended to indicate that layer 15 is thicker than layer 14. Support for these changes can be found in the specification at, for example, page 25, line 2 to page 26, line 8. No new matter has been added. Approval of these changes is respectfully requested.

The disclosure stands objected to based on a minor informality. Applicants have amended the specification to correct the informality as kindly suggested by the Examiner.

Claims 1-8, 21-26, 28 and 32-39 stand rejected under 35 U.S.C. § 102(b) as being anticipated by JP 3-196677 to Soeda. Claims 9, 13, 29, 30, 40 and 41 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Soeda in view of applicant's admitted prior art shown in Fig. 3. Applicants respectfully traverse these rejections.

The action alleges that Soeda shows all the features of independent claims 1, 21 and 32. As amended, claims 1, 21 and 32 each call for, among other features, a semiconductor substrate on which a plurality of transistors having gate insulation films of three or more different thicknesses are formed. As correctly noted by the action, transistors 5', 6', 12' and 13' formed on a substrate as shown in Figure 1 of Soeda have thick oxide gate insulation films in comparison to the thin oxide gate insulation films of transistors 14 and 15 formed on the substrate. Notably, Soeda fails to teach or suggest anything more than gate insulation films of two differing thickness. Stated differently, Soeda lacks a teaching or suggestion of a semiconductor substrate on which a plurality of transistors having gate insulation films of *three or more different*

thicknesses are formed as called for in each of independent claims 1, 21, and 32. For at least this reason, claims 1, 21 and 32 are patentably distinct from Soeda. Claims 2-8, 22-28 and 33-39, which ultimately depend from claims 1, 21 and 32, respectively, are patentably distinct from Soeda for the same reasons as their ultimate base claim and in further of the advantageous features recited therein.

Figure 3 of applicants' invention fails to overcome the above noted deficiency of Soeda. Thus, the combination of Soeda and applicants' Figure 3, even if proper, does not result in the invention of claims 9, 13, 29, 30, 40 and 41. As such, claims 9, 13, 29, 30, 40 and 41 are patentably distinct from the applied art.

CONCLUSION

It is believed that no fee is required for this submission. If any fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733, accordingly.

All rejections having been addressed, applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicit prompt notification of the same.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: November 23, 2004

By: 

Gary D. Fedorochko
Registration No. 35,509

1001 G Street, N.W.
Washington, D.C. 20001-4597
Tel: (202) 824-3000
Fax: (202) 824-3001

GDF:lab